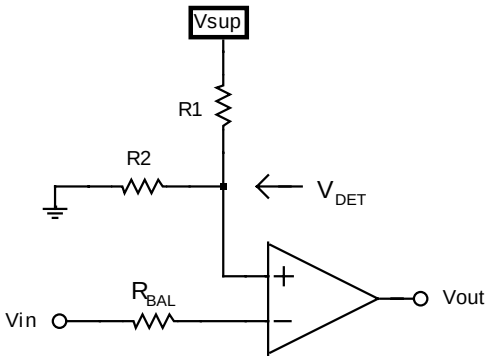
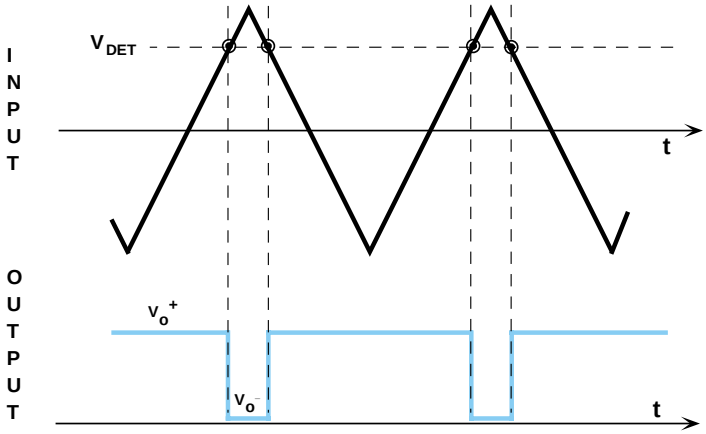
LEVEL DETECTORS AND SCHMITT TRIGGERS

INTRODUCTION

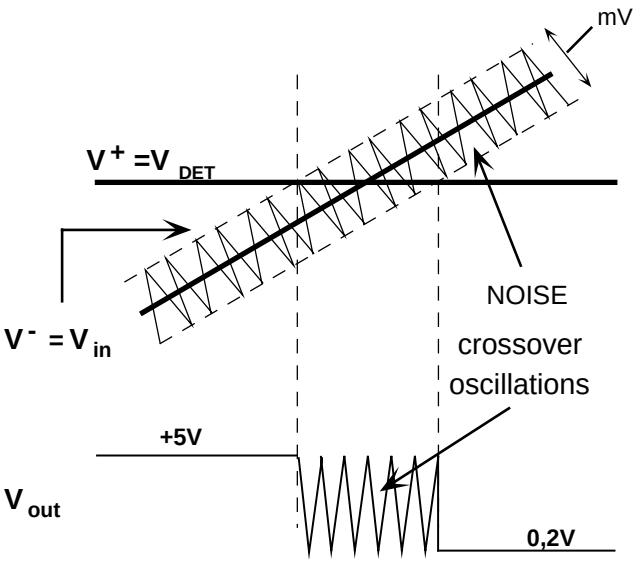
A level detector can be implemented very simply with a voltage comparator as shown below. The voltage level to be detected is generated with a voltage divider and applied either to the positive or negative input and the analog signal is applied to the other input. Voltage comparators are op amps that are not internally stabilised for negative feedback in order to provide a faster operation - smaller rise and fall times of O/P. Voltage comparators can also provide logic compatible voltage levels at their O/P. Normal op amps can be used if slower operation can be tolerated but the O/P saturation levels are usually not logic level compatible except for a few op amps.

Ideally the output waveform of a voltage comparator will be as shown below where the output level tells whether the input signal is above or below the detection level set up at one of the comparator inputs.



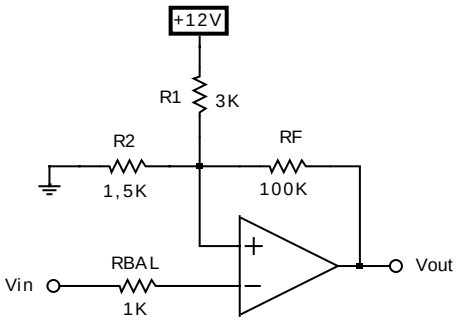


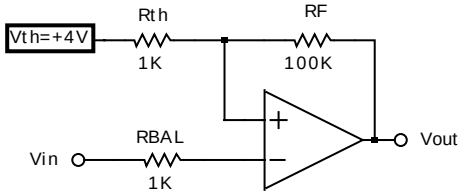
In practice, any substantial noise appearing on the input signal will make the O/P oscillate or "chatter" when the input signal is in the vicinity of the detection level. Even without noise, the O/P may chatter because of undesired negative feedback usually caused by stray capacitance or undesired negative feedback through the supply rails. To minimise feedback through supply rails, by-pass capacitors should be connected right next to supply pins. The input signal should be filtered as much as possible to reduce the noise level.



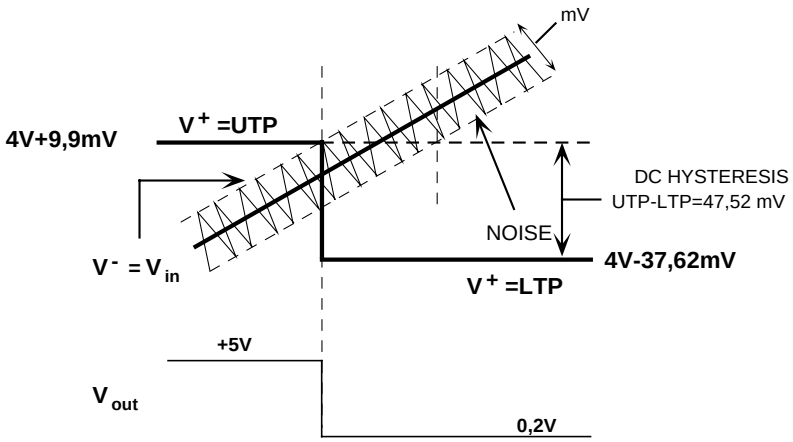
Elimination of Chattering by Use of Positive Feedback

First method: DC coupled positive feedback or DC hysteresis





Use of positive feedback will produce a voltage step in the detection threshold to pull the +ve input voltage out of reach of the -ve input voltage (input signal + noise here for inverting detector) thus forcing the output to switch only once. This will work as long as the peak to peak noise voltage is less than the hysteresis voltage or voltage step.



$$V^+ = V_o \times \frac{R_{TH}}{R_{TH}+R_F} + V_{TH} \times \frac{R_F}{R_{TH}+R_F} = V_o \times \frac{1K}{1K+100K} + 4 \times \frac{100K}{100K+1K} = 3{,}96 + \frac{V_o}{101}$$

For design purposes, use

$$\frac{R_F}{R_{TH}} = \frac{\Delta V_o}{UTP - LTP} - 1 = \frac{\Delta V_o}{\Delta V^+} - 1$$

where ΔV^+ is the hysteresis or noise margin.

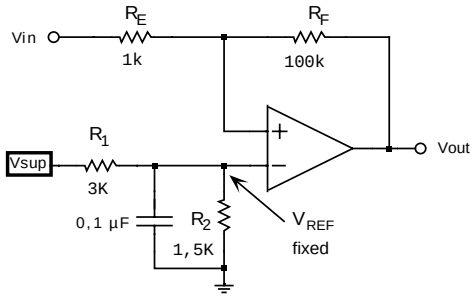
$$V^+ = UTP = 3{,}96 + \frac{V_o^+}{101} = 3{,}96 + \frac{5}{101} = 4{,}01V$$

$$V^+ = LTP = 3{,}96 + \frac{V_o^-}{101} = 3{,}96 + \frac{0{,}2}{101} = 3{,}962V$$

$$Hysteresis \quad UTP - LTP = 4{,}01 - 3{,}962 = 48\,mV$$

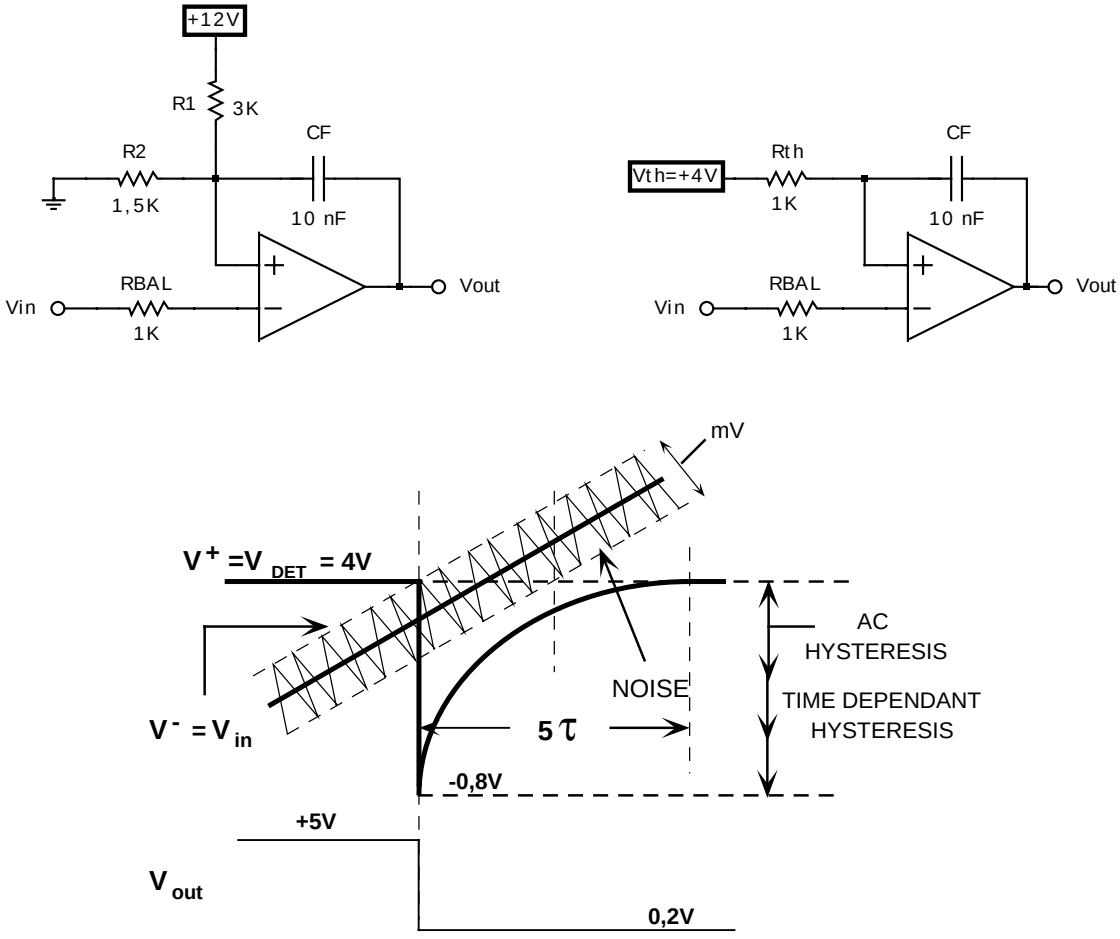
Non-Inverting Detector

Positive feedback can also be used with the non-inverting comparator to get rid of chattering, the only difference being that the reference voltage is kept fixed at the -ve I/P and V^+ is not a low amplitude squarewave superimposed on the detection level but it is a small amplitude squarewave superimposed on top of a fraction of V_{in}.



$$V^+ = V_o \times \frac{R_E}{R_E+R_F} + V_{in} \times \frac{R_F}{R_E+R_F} = V_o \times \frac{1K}{1K+100K} + V_{in} \times \frac{100K}{100K+1K} = 0{,}99V_{in} + 0{,}0099V_o$$

Second method: AC coupled positive feedback or AC hysteresis



The output will switch cleanly, only once, upon detecting the threshold voltage set up by the voltage divider R_1-R_2 as long as the hysteresis voltage or differential voltage V^+-V^- is kept greater than the noise voltage present at the input. The feedback capacitor only provides a temporary +ve feedback pulse which pulls V^+ out of reach of V^- for about 5τ for low level noise. The worst case scenario will occur when the slope of the input signal is the lowest, that is when (V_{in}+noise) takes the longest time to cross the detection threshold.

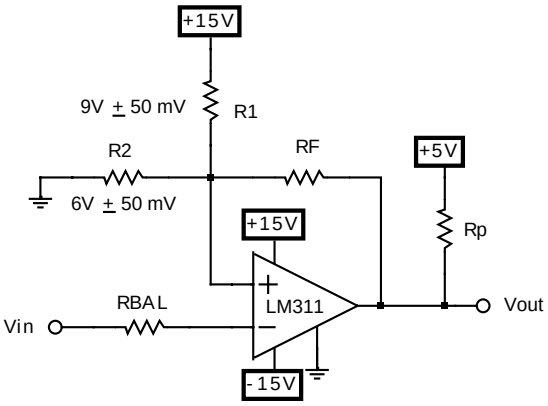
For low-level noise: $$5\tau \rangle \frac{\Delta V_{in}}{(dV_{in}/dt)_{\min}} = \frac{noise\ \ m\arg in}{\min.\ slope}$$ where $\tau = R_{TH}\, C_F$

To be safe, one should at least double the minimum time constant obtained from the above equation.

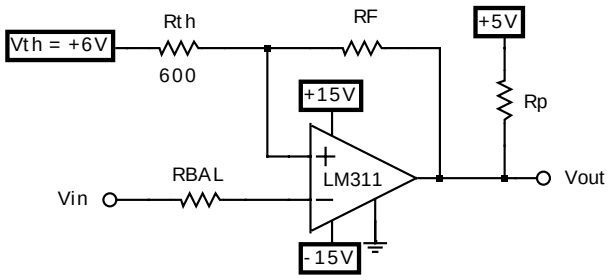
NOTE: The non-inverting configuration is not recommended because it may be inaccurate in some situations, therefore avoid using it unless you know what you are doing.

DESIGN EXAMPLE-1 LEVEL DETECTOR WITH DC HYSTERESIS

Design a +6V inverting level detector with 100 mV DC hysteresis (or 100 mV noise margin) using an LM311. The output must be TTL compatible and supply voltages available are +5V and ±15V. Analyse your circuit for exact trigger points and modify to center hysteresis exactly on +6V.



Thevenised Circuit



1. Let R_P = 1K Low R_P yields small rise time of O/P.

2. For small hysteresis values, $R_F >> R_1||R_2$ therefore let us ignore R_F and assume that it does not load the voltage divider R_1-R_2. A +6V reference voltage is set up at the +ve I/P and requires a resistor ratio $R_1/R_2 = V_1/V_2 = 9/6 = 1,5$ Let R_1 = 1,5K and R_2 = 1K std.

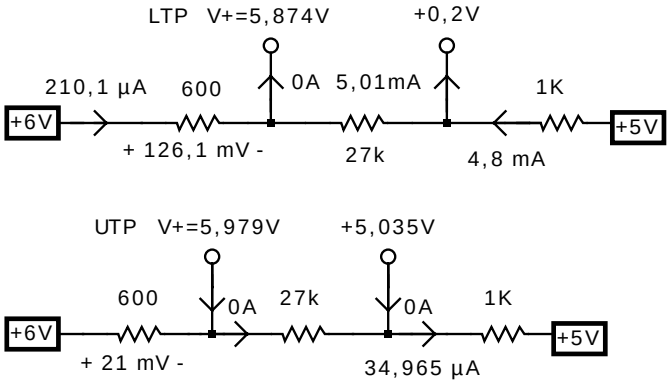
3.

$$\Delta V^+ = \Delta V_{in} = \Delta V_o \times \frac{R_{TH}}{R_{TH}+R_F} \quad \Rightarrow \quad \frac{R_F}{R_{TH}} = \frac{\Delta V_o}{\Delta V_{in}} - 1 = \frac{V_o^+ - V_o^-}{UTP - LTP}$$

$$\frac{R_F}{R_{TH}} = \frac{\Delta V_o}{\Delta V_{in}} - 1 = \frac{5-0,2}{100m} - 1 = 47 \quad \Rightarrow \quad R_F = 47 \times 1K \| 1,5K = 28,2K$$

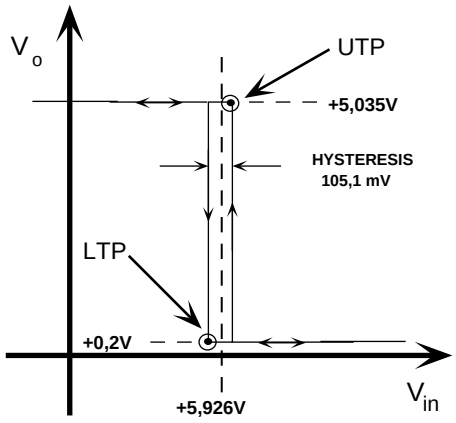
Let R_F = 27K std $R_{BAL} = 1K \| 1,5K \| 27K = 587$ (560Ω std)

4. Analysis of trigger points



LTP = 5.874V and LTP = 5.979V ave TP= 5.926V
Hysteresis = UTP - LTP = 105.1 mV

Transfer Function



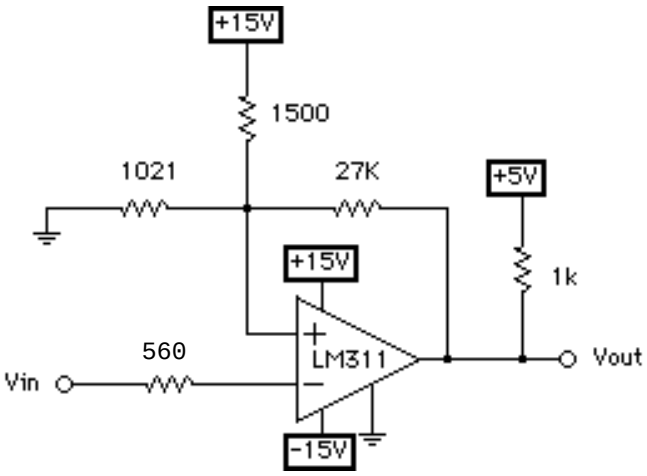
5. Design modifications

The results obtained with the preceding design are quite satisfactory for most applications where the average trigger level needs not be extremely accurate. It was assumed that R_F did not load the R_1 - R_2 voltage divider and this accounts for the average trigger level not being exactly +6V.

Now let us assume that we want an average threshold level of exactly +6V, that is we want the hysteresis curve to be centered exactly on +6V. For a good design we should derive the reference voltage from a precision voltage reference and not the +15V supply rail. Nevertheless let us assume that the +15V suplly voltage is extremely accurate and derive the reference voltage from it.

As it stands now, with R_1 = 1,5K and R_2 = 1K, the average trigger level is 5,926V and is short of +6,00V by 74 mV, therefore we need to increase the Thevenin voltage by that amount in order to center the hysteresis on 6,00V. Let us modify R_2 slightly to obtain $V_{TH} = V_2 = 6{,}074V$
$R_1/R_2 = V_1/V_2 = (15\text{-}6.074)/6.074 = 1.46954$, therefore $R_2 = 1{,}5K/1.46954 = 1021\Omega$

Final circuit



Exercise

Analyse the circuit yourself to verify that the average of the two trigger points is exactly +6,00V now and that the hysteresis is slightly higher than before.

DESIGN EXAMPLE-2 MULTI-LEVEL DETECTOR

Design a multi-level detector that fulfills the following functions. Use LM339 QUAD comparators. Comparator O/P's must be TTL compatible.

Analog I/P conditions	Binary O/P (B_1B_0)	Hysteresis on trigger levels
V_{in} > +9V	11	30 mV
+9V > V_{in} > +6V	10	30 mV
+6V > V_{in} > +3V	01	30 mV
V_{in} < +3V	00	30 mV

1. Set up a voltage divider to generate the threshold levels of +3V, +6V and +9V. Since the hysteresis is very small, the R_F values will be very high, therefore assume that the R_F's will not load the voltage divider. Filter the supply voltage to produce clean threshold voltages.

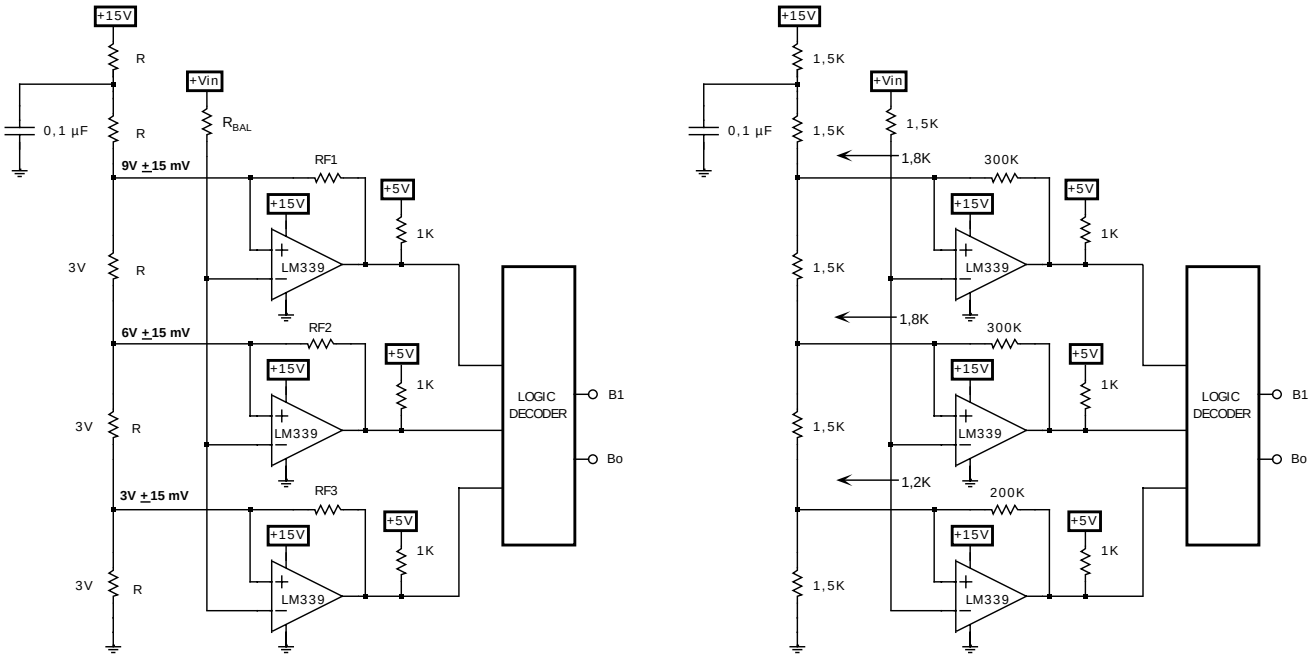
2. Determine R_{EQ} seen by +ve inputs of each comparator and calculate R_F values.

For +9V and +6V comparators, we have $R_{EQ} = 4,5K \| 3K = 1,8K$

$$\frac{R_F}{R_{EQ}} = \frac{\Delta V_0}{\Delta V_{in}} - 1 = \frac{5-0}{30m} - 1 = 165,7 \quad \Rightarrow \quad R_F = 165,7 \times 1,8K = 298,2K \rightarrow 300K \; std$$

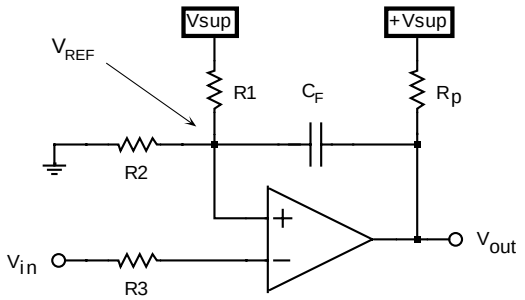
For +3V comparator, we have $R_{EQ} = 1,5K \| 6K = 1,2K$

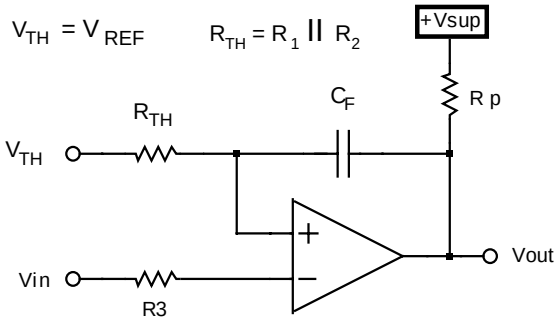
$$\frac{R_F}{R_{EQ}} = \frac{\Delta V_0}{\Delta V_{in}} - 1 = \frac{5-0}{30m} - 1 = 165,7 \quad \Rightarrow \quad R_F = 165,7 \times 1,2K = 198,8K \rightarrow 200K \; std$$



NOTE: The voltage comparators can also be connected in the non-inverting configuration.

INVERTING LEVEL DETECTOR DESIGN PROCEDURE - AC HYSTERESIS

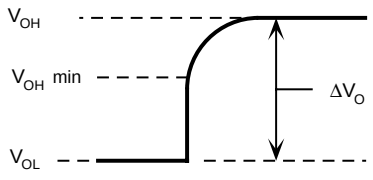




1. Pull-up resistor: with open collector devices, select value small enough for good switching speed (turn off time proportional to $R_P\ C_{stray}$)and not too small not to overload the device O/P.

2. If R_P is used, determine R_{TH} min required for valid V_{OH} on LO-HI rising edge. Use equation shown beside.

$$\left(\left[V_{OH} - V_{OL} \right] \times \frac{R_{TH}}{R_{TH} + R_P} \right) + V_{OL} \rangle V_{OH\,(\min)}$$



3. Without pull-up, determine ratio $R_2/R_1 = V_2/V_1 = \alpha$ required to obtain the desired reference voltage, then select standard R_1 and R_2 values for an accurate ratio.

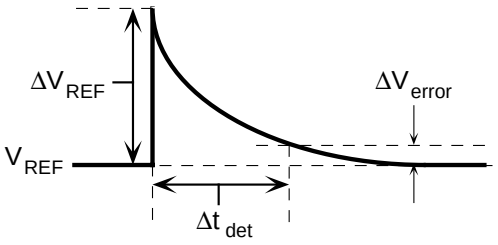
4. With pull-up resistor, determine ratio $R_2/R_1 = V_2/V_1 = \alpha$ to obtain the desired reference voltage, and then calculate R_1 min (from equation shown beside) to achieve V_{OH} min. Select standard values for best ratio of R_2/R_1.

$$\frac{1}{R_1} + \frac{1}{R_2} = \left[\frac{1}{R_1} + \frac{1}{\alpha R_1} \right] \langle \frac{1}{R_{TH\,\min}}$$

5. Calculate minimum C_F for noise margin:

$$R_{TH} C_F \rangle 0{,}5 \times noise\ margin\ /\ \left(dV_{in}/dt \right)_{\min}$$

Do not select C_F too much above limit as it restrains the minimum time between two consecutive detections. One must allow C_F to discharge between two detections, otherwise the + input of the comparator will not have time to settle back to the reference level. Use formulas shown below to determine maximum C_F given Δt_{det} minimum. If R_P is not used, then R_P=0 in formulas.



$$\Delta V_{REF} = \Delta V_O \uparrow \times \left[R_{TH} / \left(R_{TH} + R_P \right) \right] \qquad \Delta V_{REF} = \Delta V_O \downarrow$$

$$\Delta t_{det} \rangle \left(R_{TH} + R_P \right) C_F \times \ln \left[\frac{\Delta V_O \uparrow}{\Delta V_{error}} \times \frac{R_{TH}}{R_{TH} + R_P} \right] \qquad \Delta t_{det} \rangle R_{TH} C_F \times \ln \left[\frac{\Delta V_O \downarrow}{\Delta V_{error}} \right]$$

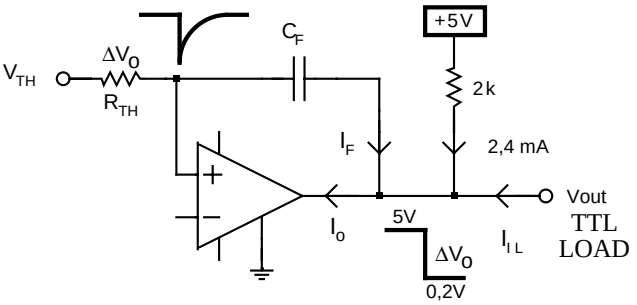
6. Make $R_3 = R_1 \| R_2$ for minimum DC offset. Select standard R_3 (not critical).

DESIGN EXAMPLE 3 Design a +6V level detector that produces a TTL output using an LM311 voltage comparator with ±15V and +5V supply voltages. Assume that the input signal is a triangular wave with an amplitude of $8V_p$ and a frequency range of 1 kHz to 25 kHz. Assume a noise margin of 20 mV and a residual voltage error of 50 mV maximum on the feedback capacitor.

1. Let R_P = 2K for fast switching of LM311 output. The maximum I_O of the LM311 will occur when the O/P switches HI to LO, and is given by the following:

$$I_{o\,(\max)} = 2,4m + I_{IL(\max)} + \Delta V_o / R_{TH}$$

where I_{IL} and $\Delta V_o/R_{TH}$ arer not known yet but will be less than 10 mA which does not pose any problem for the LM311 current capacity.

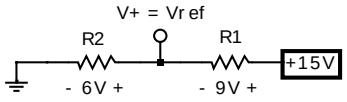


2. V_{OH} min is about 2,2V for TTL and assuming V_{OL} = 0,2V and V_{OH} = 5V for LM311, we have:

$$\left(\left[V_{OH} - V_{OL}\right]\times\frac{R_{TH}}{R_{TH}+R_P}\right)+V_{OL} \rangle V_{OH\,(\min)} \qquad \left(\left[5-0,2\right]\times\frac{R_{TH}}{R_{TH}+2K}\right)+0,2 \rangle 2,2 \quad\Rightarrow\quad R_{TH} \rangle 2,8K$$

3. N/A

4. $\dfrac{R_1}{R_2} = \dfrac{V_1}{V_2} = \dfrac{9}{6} = 1,5 \qquad \dfrac{1}{R_1}+\dfrac{1}{R_2} = \left[\dfrac{1}{R_2}+\dfrac{1}{1,5R_2}\right] \langle \dfrac{1}{2,8k} \quad\Rightarrow\quad R_2 \rangle 4,66\overline{6}k$



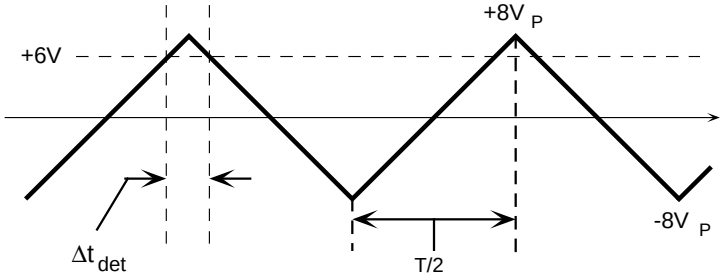
Let R_2 = 10K and R_1 = 15K for an exact ratio of 1,5

5.

$$\frac{dV_{in}}{dt}_{\min} = \frac{16V_{PP}}{0,5ms} = 32K\,V/s$$

$$\frac{dV_{in}}{dt}_{\max} = \frac{16V_{PP}}{20\mu s} = 800K\,V/s$$

$$\Delta t_{\det\ \min} = 2\times\frac{(8V-6V)}{800K\,V/s} = 5\,\mu s$$



F = 1 kHz to 25 kHz, T/2 = 20 µs to 0,5 ms

$$C_F \rangle \frac{0,5\times noise\ margin}{R_{TH}\times\frac{dV_{in}}{dt}_{\min}} = \frac{0,5\times 20mV}{6K\times 32K} = 52\ pF$$

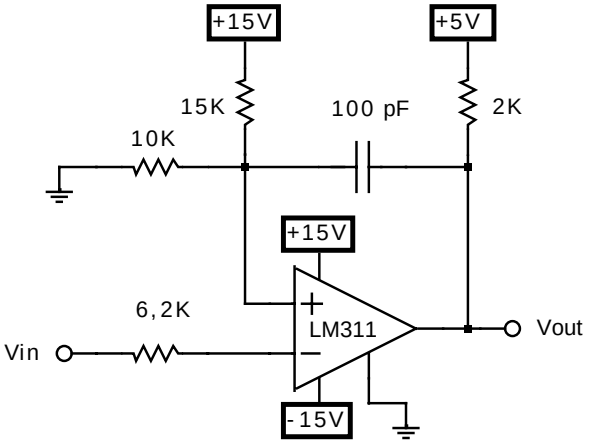
$$C_F \langle \frac{\Delta t_{\det}}{\left(R_{TH}+R_P\right)\times\ln\left[\frac{\Delta V_O\uparrow}{\Delta V_{error}}\times\frac{R_{TH}}{R_{TH}+R_P}\right]} = \frac{5\ \mu s}{(6k+2k)\times\ln\left[\frac{4,8V}{50mV}\times\frac{6k}{6k+2k}\right]} = 146,1\ pF$$

$$C_F \langle \frac{\Delta t_{\det}}{R_{TH}\times\ln\left[\frac{\Delta V_O\downarrow}{\Delta V_{error}}\right]} = \frac{5\ \mu s}{6k\times\ln\left[\frac{4,8V}{50mV}\right]} = 182,6\ pF$$

C_F = (52p + 146,1p)/2 = 99 pF, 100 pF std

6. $R_3 = R_1 \| R_2 = 10k \| 15k = 6k \quad \Rightarrow \quad 6,2k\ std$

Final circuit

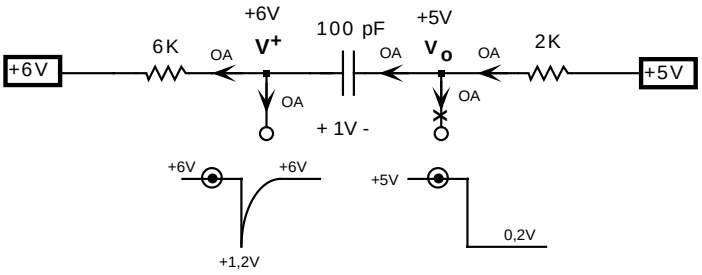


Circuit Analysis

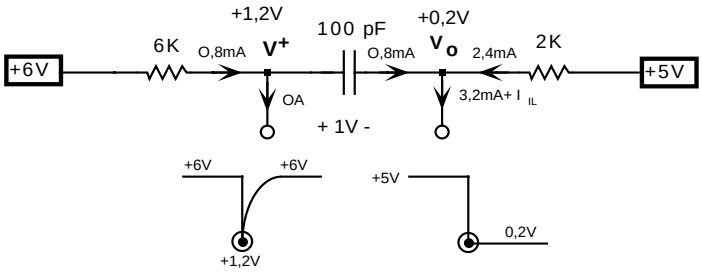
A) Analysis of falling edge

Thevenising the 10K-15K voltage divider, we obtain the circuit shown below.

Right before the falling edge, there is no current in the capacitor because it is charged at a constant voltage (i=C dV/dt). The O/P of the comparator is O/C (open circuit) therefore there is no current in the pull-up resistor if the TTL load does not draw any current.

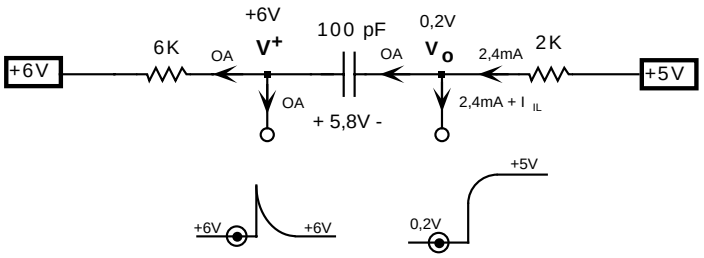


At the very instant that V_o drops from 5V to 0.2V, V^+ also drops by the same amount because the capacitor voltage does not change instantaneously but it will be charged from 1V to 5,8V in 5*6k*100p=3µs. After 5τ V^+ goes back to +6V to be ready for the next detection.

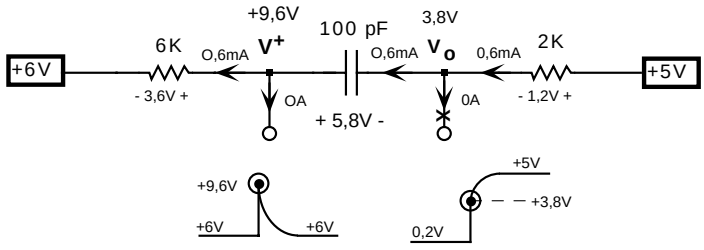


B) Analysis of rising edge

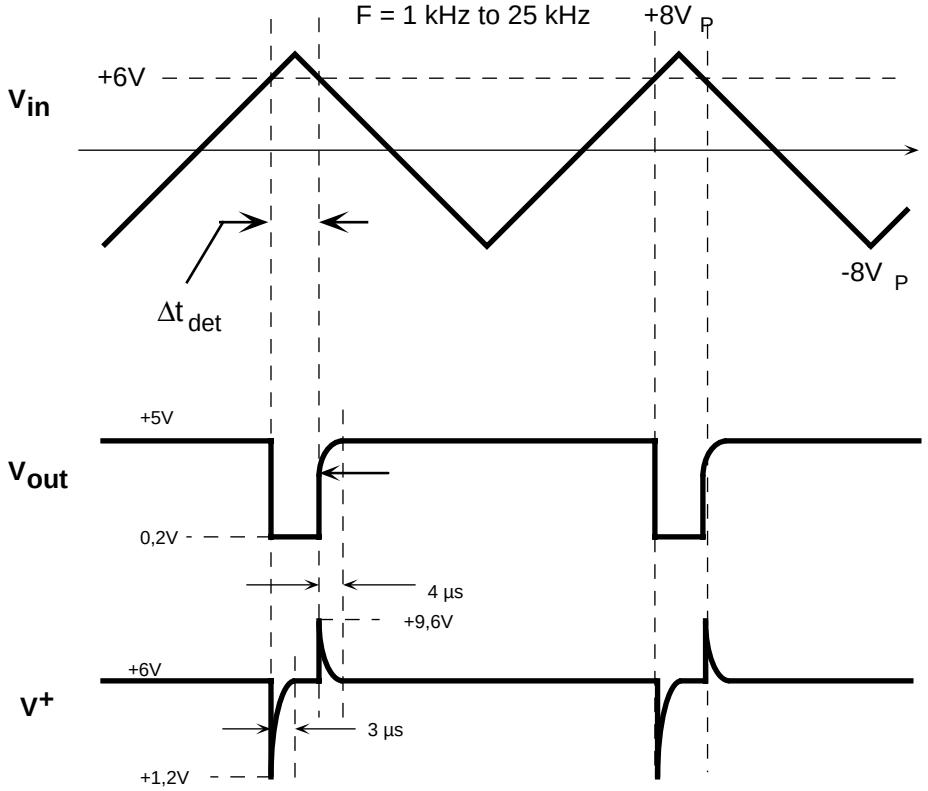
Right before the rising edge, there is no current in the capacitor because it is charged at a constant voltage (I = C dV/dt). The O/P of the comparator is saturated at about 0,2V and sinks 2,4 mA + I_{IL}. The capacitor is charged at a steady 5,8V.



At the very instant that V_o switches to a high, the O/P of the comparator goes O/C and steps up to 3,8V then rises exponentially to +5V in 5τ. The capacitor voltage does not change instaneously but the capacitor will be discharged from 5,8V to 1V in 5*(6k+2K)*100p=4 µs. After 5τ, V^+ goes back to +6V to be ready for the next detection.



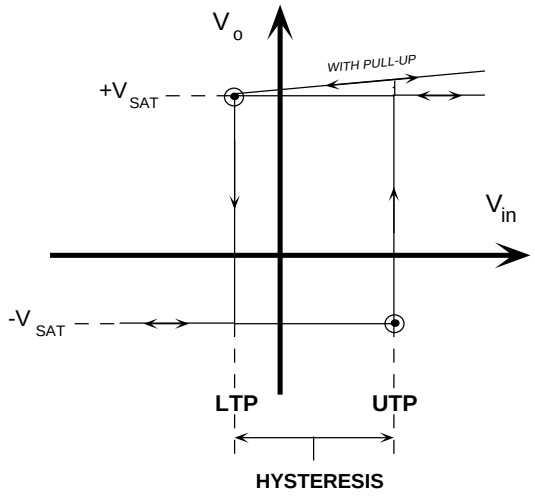
C) Overall waveforms



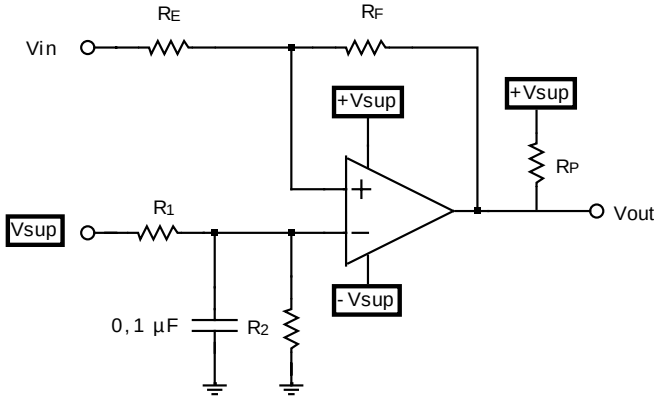
NOTE: A non-inverting level detector with AC hysteresis (capacitive feedback) is not recommended because of its poor accuracy under certain conditions.

NON-INVERTING SCHMITT TRIGGER DESIGN PROCEDURE - DC HYSTERESIS

Transfer function



Circuit diagram



V⁻ is a fixed reference voltage - 0,1 µF cap filters supply noise.

1. With open collector voltage comparators, select pull-up resistor small enough for good switching speed (turn off time α R_P C_{stray})and not too small not to overload the O/P.

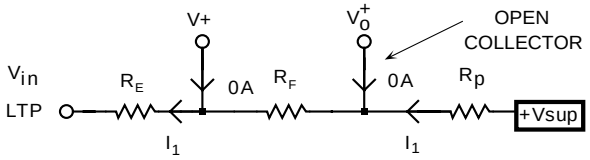
2. Calculate the ratio $\frac{R_F}{R_E} = \frac{V_o^+ - V_o^-}{UTP - LTP} = \beta$ With pull-up resistor, assume V_o^+.

3. A) With op amp, select standard R_F and R_E values large enough so that op amp O/P is not overloaded and not too large - range 10k to 500k.

B) With pull-up resistor, determine R_E+R_F necessary to obtain assumed V_o^+.

$R_E + R_F = (V_o^+ - LTP)/I \Rightarrow I = (V_{SUP} - V_o^+)/R_P$

ratio $R_F/R_E = \beta$



Solve above two equations for $R_{E\ (theo)}$ then try standard values around $R_{E(theo)}$ to achieve R_F/R_E ratio.

4. Using standard values of R_E and R_F analyze the circuit in order to find the reference voltage needed by assuming $V^+ = V^-$ at one of the trigger points.

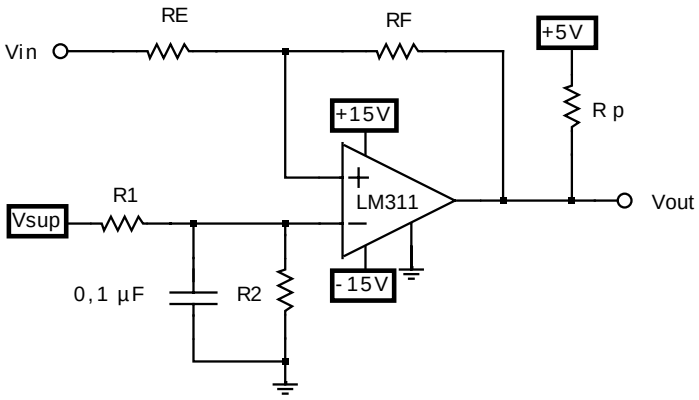
5. Calculate ratio $R_1/R_2 = V_1/V_2 = \alpha$ for desired V_{REF}

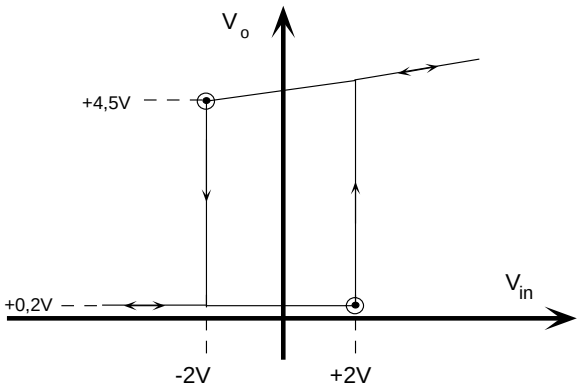
A) FET input op amp or comparator: determine standard values of R_1 and R_2 needed to obtain the reference voltage.

B) BJT input op amp or comparator: ratio R_1/R_2 and approximate balancing of the DC input resistance (for min DC offset) is required.

$\frac{1}{R_1} + \frac{1}{R_2} = \left[\frac{1}{R_E} + \frac{1}{R_F} = \frac{1}{\alpha R_2} + \frac{1}{R_2}\right] \Rightarrow$ solve for $R_{2(theo)}$, then try several standard values around $R_{2(theo)}$ and select best R_1 - R_2 combination for an accurate ratio α.

DESIGN EXAMPLE 4 NON-INVERTING SCHMITT TRIGGER





Design a Schmitt trigger with the hysteresis function shown above. Use R_P = 1,5K.

1. R_P = 1,5K

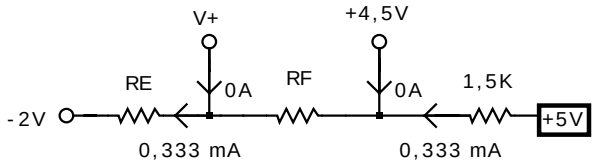
2. $$\frac{R_F}{R_E} = \frac{V_o^+ - V_o^-}{UTP - LTP} = \frac{4.5 - 0.2}{2 - (-2)} = 1.075 = \beta$$

3. N/A

4.

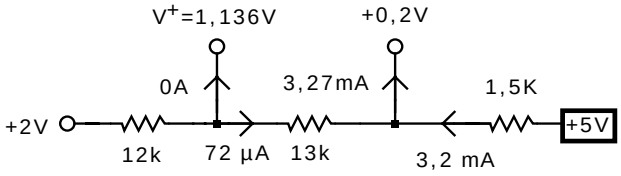
$$R_E + R_F = \frac{4,5 - (-2)}{0,333m} = 19.5K = R_E + 1.075R_E$$

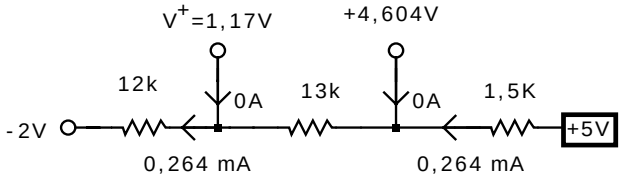
$$2.075R_E = 19.5K \quad \Rightarrow \quad R_E = 9.4K$$



R_E std	8.2k	9.1k	10k	11k	**12k**
$R_F = 1.075R_E$	8.82k	9.78k	10.75k	11.82k	**12.9k**
R_F std	9.1k	10k	11k	12k	**13k**

5. Analyse for V_{REF} required - use either one of the two trigger points.





One can see that $V_{REF} = V^+$ is not exactly the same for both trigger points because the standard resistor values are not equal to the theoretical values.

V_{REF} ave = (1,17+1,136)/2 = 1,153V

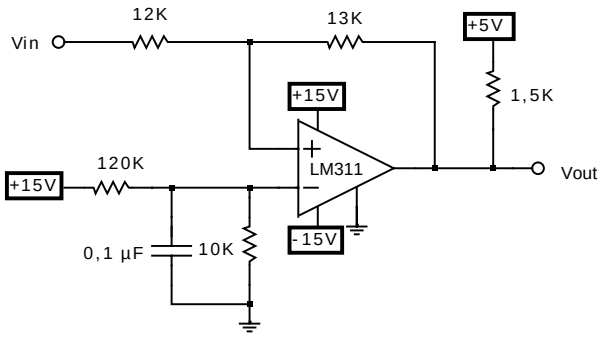
6. $\frac{R_1}{R_2} = \frac{V_1}{V_2} = \frac{15 - 1.153}{1.153} = 12.01$ To balance the inputs for minimum DC offset, we have:

$$\frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{12.01R_2} + \frac{1}{R_2} = \frac{1.0833}{R_2} = \frac{1}{12K \| 13K} \quad \Rightarrow \quad R_2 = 6.76K$$

Select standard R_1 and R_2 for an accurate ratio with an R_2 value picked around 6.76K.

R_2 std	5.6k	6.2k	6.8k	7.5k	8.2k	**10k**
$R_1 = 12\ R_2$	67.2k	74.4k	81.6k	90k	98.4k	**120k**
R_1 std	68k	75k	82k	91k	100k	**120k**

Final Circuit

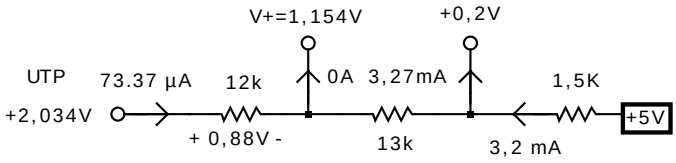


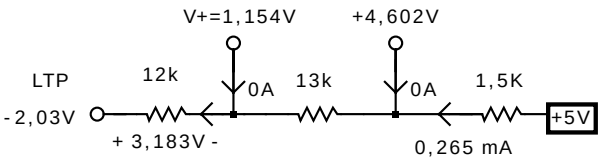
Note: The two input resistances are not perfectly balanced, that is R_P = 6.24K and R_N = 9.23K, which cause a small offset of the trigger points (x mV) but this does not pose a major problem if the accuracy of the trigger points is not too critical.

CIRCUIT ANALYSIS

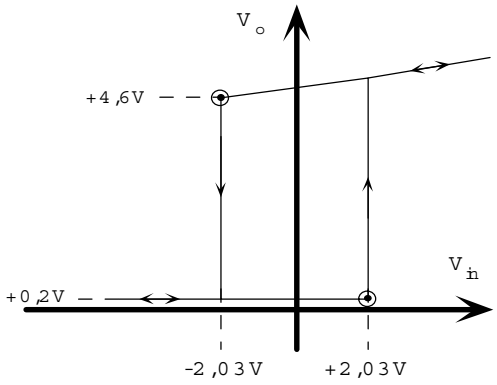
First find the reference voltage and then find the two input voltages for which $V^- = V^+ = V_{REF}$.

V_{REF} = 15 x 10k / (10K +120K) = 1,154V

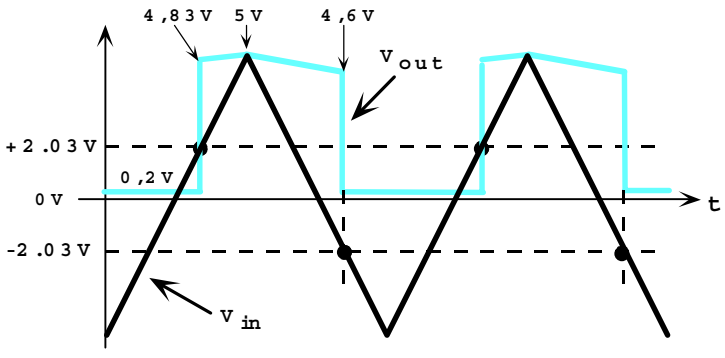




Transfer function



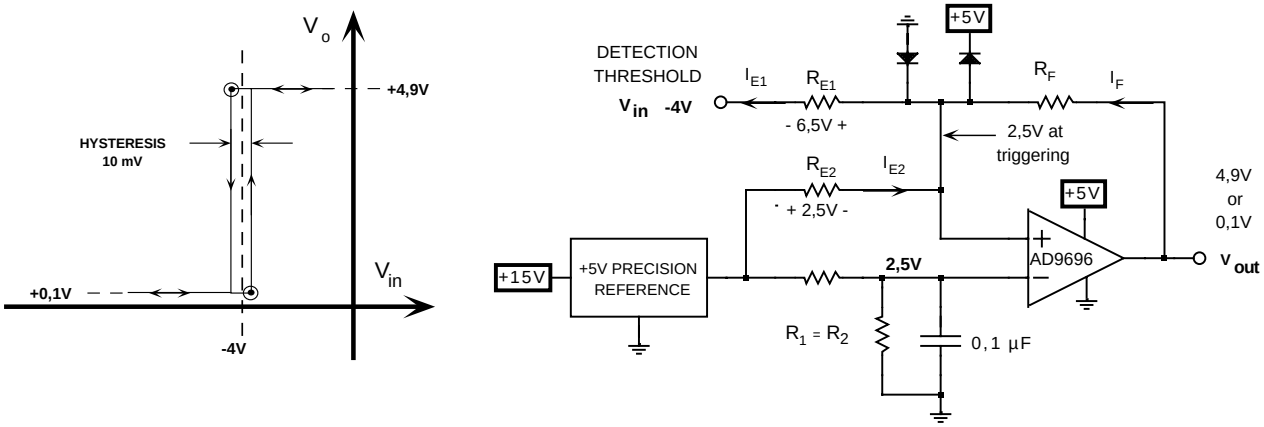
Waveforms



NOTE: One can notice that V_{out} varies a little with V_{in} in the high state because of the open collector O/P of the LM 311: $V_o = 5 \times \frac{R_E + R_F}{R_E + R_F + R_E} + V_{in} \times \frac{R_P}{R_E + R_F + R_E} = 4,717 + 0,0566\ V_{in}$

DESIGN EXAMPLE 5 HI-SPEED LEVEL DETECTOR WITH DC HYSTERESIS

Design a threshold detector for a detection level of -4V and a 10 mV hysteresis using a Schmitt trigger. Use a high speed AD9696 voltage comparator with +5V supply. Use a +5V precision voltage reference powered off a +15V supply for an accurate threshold.



AD9696 DATA V_{SUP} = ±7V max V^- and V^+ = ±5V max $V^- - V^+$ = ±5,4V max
input voltage range: +1,4V to 3,7V with V_{SUP} = +5V and 0V
output voltage levels: V_{OL}=0,1V and V_{OH}=4,9V typical at no load
propagation delay: 4,5 ns typ, 7 ns max
input bias current: 16 µA typ, 55 µA max at 25°C

We cannot apply -4V directly to the comparator inputs with a single +5V supply because the input voltage range is restricted from +1,4V to +3,7V with a midrange value of 2,55V. Therefore we will have to pull up the input trigger voltage of -4V to some arbitrary value within the input range. Let us pick $V^+ = V^- = +2{,}5V$ at triggering which makes it easy to derive from the +5V reference, that is $R_1 = R_2$.
Because the hysteresis is so small, $R_F >> R_{E1} \| R_{E2}$ and $I_F << I_{E1}$ or I_{E2}, therefore $I_{E1} \approx I_{E2}$.

From the circuit diagram, we have: $$\frac{R_{E1}}{R_{E2}} = \frac{6,5}{2,5} = 1,6 \quad \Rightarrow \quad R_{E1} = 1,6k \; and \; R_{E2} = 1k$$

R_{E1} and R_{E2} should not be picked too large if we want maximum switching speed of the comparator because the +ve feedback voltage can be slowed down by the input stray capacitance (3 pF typ) of the AD9696 where the time constant is $\tau^+ = \left(R_{E1} \| R_{E2} \| R_F\right) C_{STRAY} \approx \left(R_{E1} \| R_{E2}\right) C_{STRAY}$.

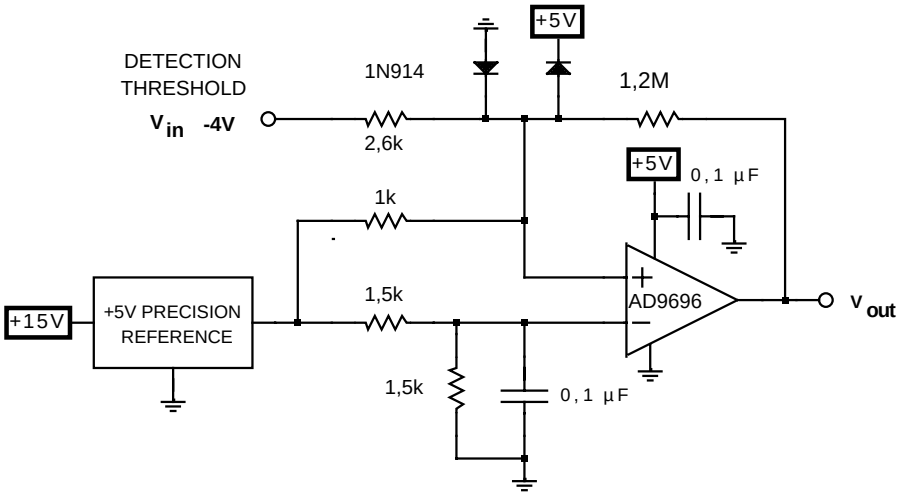
R_F is calculated for the desired hysteresis:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_{OH} - V_{OL}}{UTP - LTP} \approx \frac{R_F}{R_{E1}} = \frac{4.9 - 0.1}{10m} = 480 \quad \Rightarrow \quad R_F = 480 \times R_{E1} = 1,248M \; (1,2M \; std)$$

To balance the inputs, we have:

$$R_1 \| R_2 = 0,5R_1 = R_{E1} \| R_{E2} \| R_F = 2.6k \| 1k \| 1.2M = 722 \quad \Rightarrow \quad R_1 = R_2 = 2 \times 722 = 1.44k \quad \Rightarrow \quad 1.5k \; std$$

Tentative circuit #1



Derivation of hysteresis formula

$$At\ triggering,\ V^- = V^+ = V_{out}\frac{R_{E1}\|R_{E2}}{R_{E1}\|R_{E2}+R_F} + V_{REF}\frac{R_{E1}\|R_F}{R_{E1}\|R_F+R_{E2}} + V_{in}\frac{R_{E2}\|R_F}{R_{E2}\|R_F+R_{E1}}$$

$$Since\quad R_F \rangle\rangle R_{E1}\ or\ R_{E2} \qquad V^+ \approx V_{out}\frac{R_{E1}\|R_{E2}}{R_F} + V_{REF}\frac{R_{E1}}{R_{E1}+R_{E2}} + V_{in}\frac{R_{E2}}{R_{E1}+R_{E2}}$$

$$V_{in} = V^+\frac{R_{E1}+R_{E2}}{R_{E2}} - V_{out}\frac{R_{E1}}{R_F} - V_{REF}\frac{R_{E1}}{R_{E2}} \quad\Rightarrow\quad \Delta V_{in} = \Delta V_{out}\frac{R_{E1}}{R_F}$$

If we account for input bias currents of the comparator, we can show the following for balanced input resistances:

$$UTP - LTP = \Delta V_{in} = \Delta V_{out}\frac{R_{E1}}{R_F} - 4\ I_{BIAS}R_{E1}$$

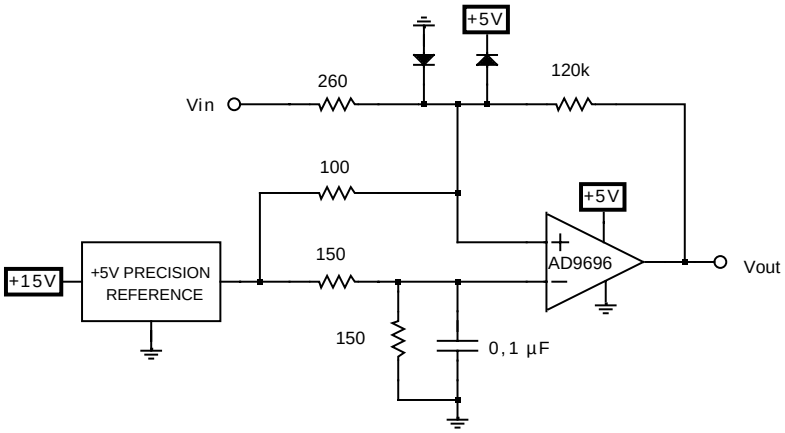
NOTE: positive I_{BIAS} for current going into inputs of comparator and negative I_{BIAS} for current coming out of comparator.

$$UTP - LTP = \Delta V_{out}\frac{R_{E1}}{R_F} - 4\ I_{BIAS}R_{E1} = (4.9-0.1)\times\frac{2.6k}{1.2M} - 4\times 16\mu\times 2.6k = 0.155V\ typ$$

$$UTP - LTP = \Delta V_{out}\frac{R_{E1}}{R_F} - 4\ I_{BIAS}R_{E1} = (4.9-0.1)\times\frac{2.6k}{1.2M} - 4\times 55\mu\times 2.6k = 0.562V\ \max$$

One can see that I_{BIAS} being so large here will cause a huge difference on the hysteresis. In order to reduce this effect we must lower all resistor values - let us reduce them by a factor of ten.

Tentative circuit #2

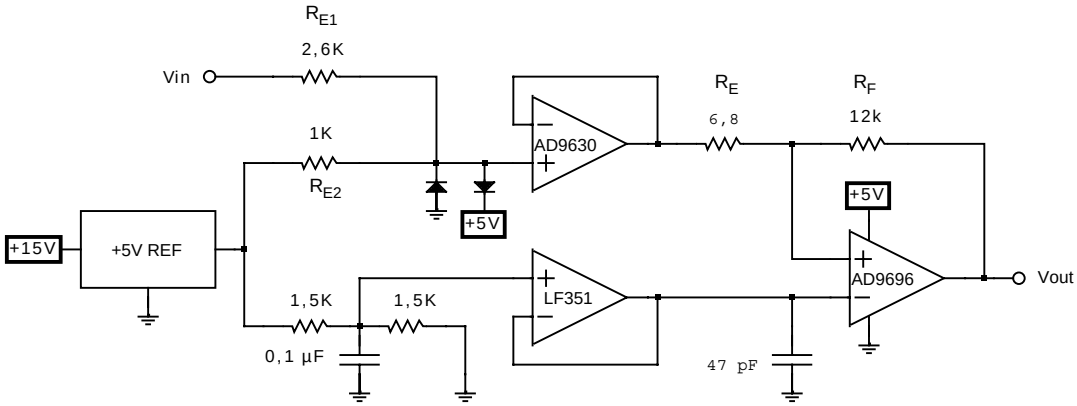


$$UTP - LTP = \Delta V_{out}\frac{R_{E1}}{R_F} - 4\,I_{BIAS}R_{E1} = (4.9-0.1)\times\frac{260}{120k} - 4\times(\pm 16\mu)\times 260 = 6{,}24\ mV\ or\ 27{,}04\ mV\ typ$$

With small resistors, the hysteresis is much smaller but somewhat unpredictable. If I_{BIAS} is positive, the hysteresis will be 6,24 mV typical, if it is negative then it will be 27.04 mV typical. Note that I_{BIAS} and V_{io} of the comparator will also modify the expected detection threshold, therefore one of the 150 resistors should be trimmed for an accurate detection threshold of -4V. The currents in the above circuit will be too large for most IC's to handle, therefore one should modify the design as shown below where the buffers allow the use of larger resistors and reasonable currents drawn from V_{in} and V_{REF}.

Final Circuit

$$\frac{R_F}{R_E} \approx \frac{\Delta V_{out}}{UTP - LTP}\times\left(1+\frac{R_{E1}}{R_{E2}}\right) = \frac{(4.9-0.1)}{10m}\times\left(\frac{1k+2{,}6k}{1k}\right) = 1728$$ if I_{BIAS} is ignored.

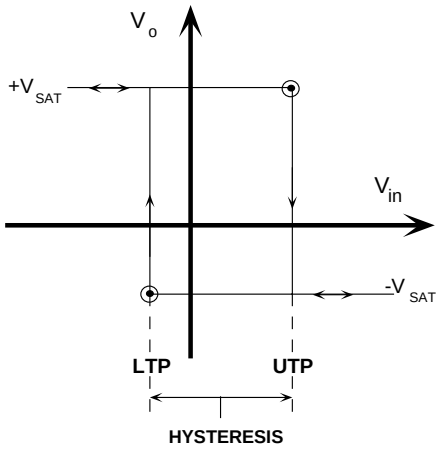


$$UTP - LTP = \left(\Delta V_{out}\frac{R_E}{R_F} \pm 2\,I_{BIAS}R_E\right)\times\frac{R_{E1}+R_{E2}}{R_{E2}}$$

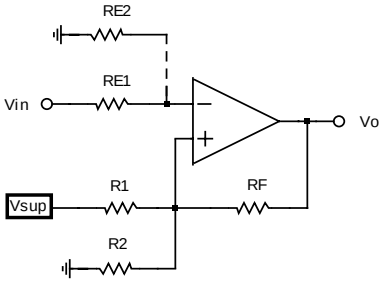
$$UTP - LTP = \left((4.9-0.1)\times\frac{6{,}8}{12k} \pm 2\times 16\mu\times 6{,}8\right)\times\left(\frac{1k+2{,}6k}{1k}\right) = \begin{matrix} 9\,mV \\ or \\ 10{,}57\,mV \end{matrix}\quad typ$$

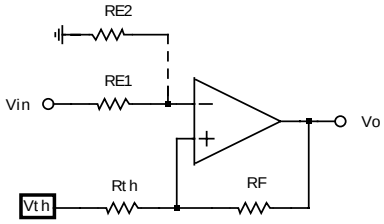
INVERTING SCHMITT TRIGGER DESIGN PROCEDURE - DC HYSTERESIS

Transfer function



Circuit diagram





Thevenin equivalent:

$$R_{TH} = R_1 \| R_2 \qquad V_{TH} = V_{SUP} \times R_2 / (R_1 + R_2)$$

1. With open collector voltage comparators, select pull-up resistor small enough for good switching speed (turn off time α R_P C_{stray})and not too small not to overload the O/P.

2. Calculate the ratio

$$\frac{R_F}{R_{TH}} = \frac{V_o^+ - V_o^-}{UTP - LTP} - 1 = \frac{\Delta V_0}{\Delta V_{in}} - 1 \;=\; \beta$$

With pull-up resistor, assume a reasonable V_o^+.

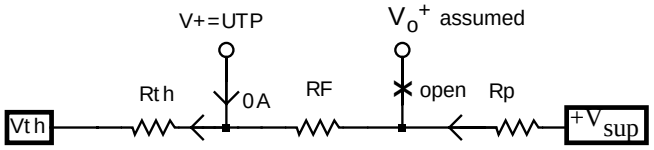
If the result is a -ve resistor ratio, V_{in} has to be attenuated with voltage divider R_{E1}-R_{E2} where

$$\frac{R_F}{R_{TH}} = \frac{V_o^+ - V_o^-}{UTP_A - LTP_A} - 1$$

and attenuated trigger points are: $UTP_A = UTP \times \dfrac{R_{E2}}{R_{E1} + R_{E2}}$ *and* $LTP_A = LTP \times \dfrac{R_{E2}}{R_{E1} + R_{E2}}$

3.A) With no pull-up, select standard R_F value large enough so that op amp O/P is not overloaded and not too large . Next calculate theo. value of R_{TH} for ratio β found in step 2.

B) With pull-up resistor, determine theo. R_F necessary to obtain assumed V_o^+ and select closest standard value. Next calculate theo. value of R_{TH} from ratio β found in step 2.



4. Using values of R_{TH} and R_F analyze the circuit to find V_{TH}.needed by assuming $V^+ = V^-$ at one of the trigger points then calculate the ratio $R_1/R_2 = V_1/V_2 = \alpha$ for the desired V_{TH}. Determine theoretical values of R_1 and R_2 for desired ratio R_1/R_2 and $R_{TH} = R_1 \| R_2$ as found in step 3.
Solving for R_2 in the equation shown beside will satisfy both conditions. Since both R_{TH} and the ratio are critical for an accurate hysteresis, select a combination of two standard resistors to achieve theoretical values of R_1 and R_2.

$$\frac{1}{R_{TH}} = \frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{\alpha\, R_2} + \frac{1}{R_2}$$

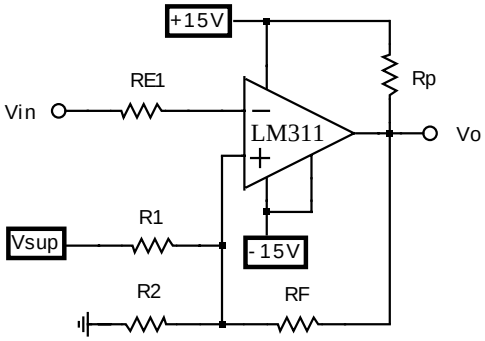
5. With single R_E, make $R_E = R_1 \| R_2 \| R_F$ for minimum DC offset. With R_{E1} and R_{E2},

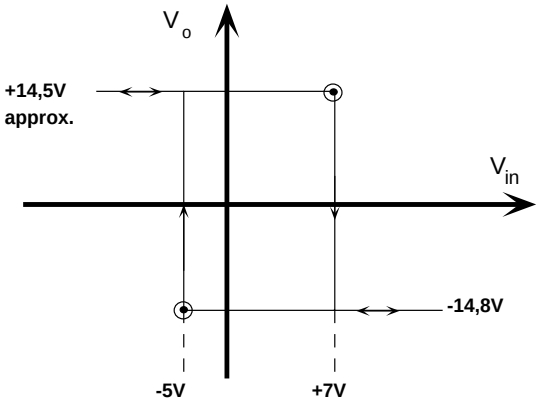
$$\frac{1}{R_{E1}} + \frac{1}{R_{E2}} = \left[\frac{1}{R_1 \| R_2 \| R_F} = \frac{1}{\gamma\, R_{E2}} + \frac{1}{R_{E2}} \right]$$

Solve for $R_{E2(theo)}$, then try several standard values around $R_{2(theo)}$ and select best R_{E1} - R_{E2} combination for an accurate ratio $\gamma = R_{E1}/R_{E2}$

DESIGN EXAMPLE 6 INVERTING SCHMITT TRIGGER

Design a Schmitt trigger witg the transfer function shown beside using an LM311 voltage comparator.



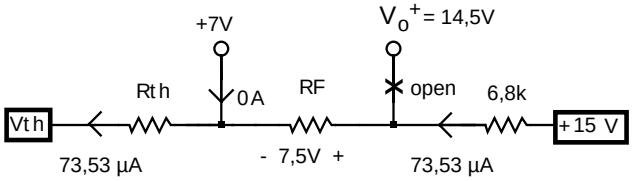


1. Let I_{Rp} = 5 mA max not to overload the LM311 output, therefore
   $R_p \geq$ (15-(-14,8))/ 5m = 5,96K, let R_P = 6,8K

2. $$\frac{R_F}{R_{TH}} = \frac{V_o^+ - V_o^-}{UTP-LTP} - 1 = \frac{14.5 - ((-14,8)}{7 - (-5)} - 1 = 1,442 = \beta$$

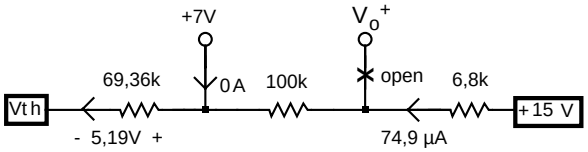
3. R_F = 7,5 / 73.53µ = 102k, 100K std

   R_{TH} = 100K / 1.443 = 69,36K



4. V_{th} = 7 - 5.19 = +1.804V

NOTE: do not assume V_o^+ = +14,5V because standard R_F is now used and
I = (15 - 7)/106,8K= 74.98 µA

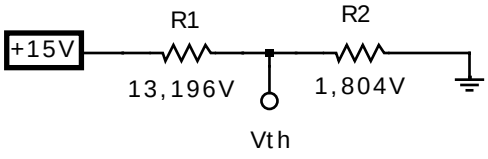


You can also use the other trigger point to find V_{TH} - result will differ slightly.

R_1 / R_2 = 13.196/1.804 = 7,314 = α

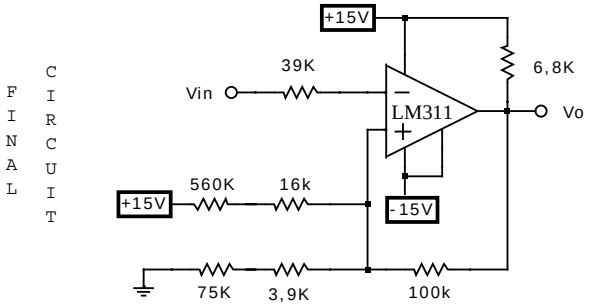
$$\frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{R_{TH}} \quad \Rightarrow \quad \frac{1}{7.314\,R_2} + \frac{1}{R_2} = \frac{1}{69,36k}$$

$$solving \quad \Rightarrow \quad R_2 = 78,84k$$

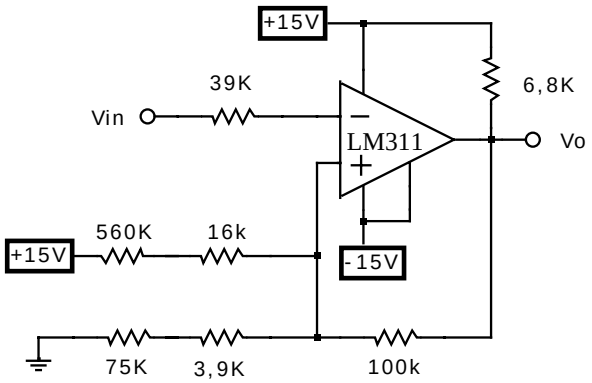


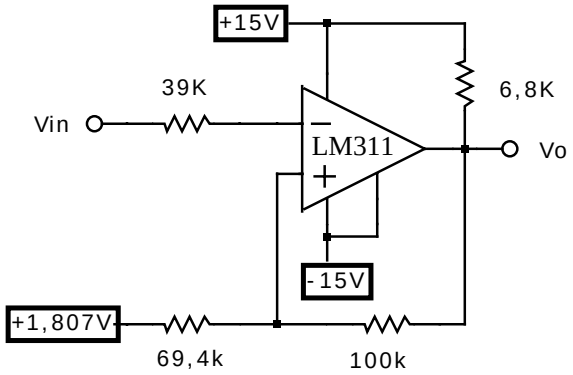
Since both R_{TH} and the ratio R_1/R_2 are important, let R_2 = 75K + 3,9K std, therefore we have R_1 = 78.9K x 7.314 = 576,6K, that is 560k in series with 16k.

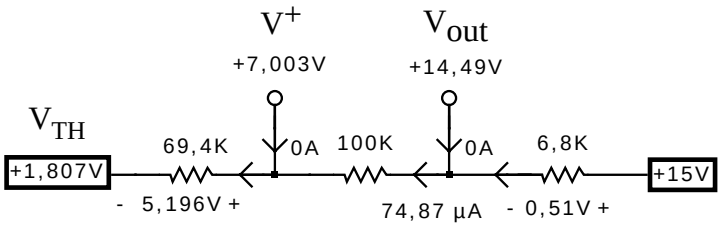
5. $$R_E = R_1 \| R_2 \| R_F = 576,6k \| 78.9k \| 100k$$
   $$R_E = 40,97k \Rightarrow 39k\ std$$

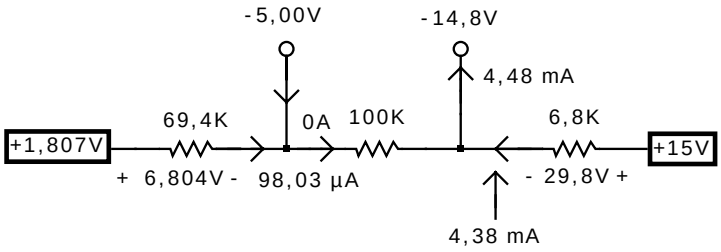


Analysis of trigger points









Waveforms